

## *Invited Talk*

# **Dis on a Chip – Design, Challenges, Implementation**

Bruce Ellis {brucee@chunder.com}

### *ABSTRACT*

Increasingly complex systems are now targeted at programmable logic chips, as they have increased in size and versatility nearly as fast as is needed, and the verification and simulation tools are becoming realistic.

The Dis VM is a particularly good fit for a FPGA, though quite a challenge.

We explore the design and implementation of the Dis VM purely in an HDL.

Applications include: PCI card running Dis using hosted resources, same card using local resources (Gbit IP), or stand-alone tiny and cheap programmable box.

Challenges are all centred on:

- 1) maximizing parallelism
- 2) avoiding dead cycles.

Cluster? Many such chips can fit on a board. More than one VM can fit on a chip. Many boards. We soon have a billion gates working for us.